REMARKS

An Office Action was mailed August 21, 2008 and was declared final. This Response is timely. Any fee due with this paper, including any necessary extension fees, may be charged on Deposit Account 50-1290.

Summary

Claims 1-3, 5, and 11-18 are pending. Claim 1 is the only independent claim.

By the foregoing, claims 1 and 5 are amended. No new matter has been added.

Rejections in view of Williams

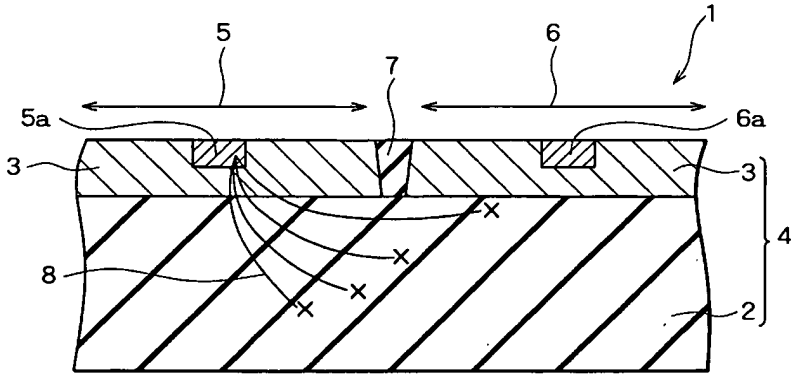
Claims 1, 5, 11-13, 16, and 18 stand rejected under 35 U.S.C. §102(b) as being anticipated by or stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,156,989 to Williams.

The presently claimed invention includes the limitations:

> *"a silicon substrate having a substantially planar top substrate surface;*
> *a silicon epitaxial layer having a lower resistivity than the resistivity of said silicon substrate, the epitaxial layer having a substantially planar lower epitaxial surface, the epitaxial layer being formed upon the top substrate surface so that the lower epitaxial surface and the top substrate surface are adjacent;*
> *a first and a second circuit section formed in said silicon epitaxial layer, each circuit section spaced apart from the top substrate surface by a respective portion of the silicon epitaxial layer; and"*

The gist of the invention is to greatly simplify producing a reduced noise circuit and such a circuit. As can be seen in Fig. 3 of the application, the silicon substrate 2 includes a substantially planar top surface upon which an epitaxial layer is formed so that a substantially planar lower epitaxial surface and the top substrate surface are adjacent. See, for example, 8:14-17 wherein

CVD deposition results in planar surfaces. Diffusion layers 5a and 6a, which are the respective digital or analog circuit section (see 9:6-7), are spaced apart from a top surface of the silicon substrate 2 by a portion of the epitaxial layer.



Since the epitaxial layer 3 *"[has] a lower resistivity than the resistivity of said silicon substrate"* the analog and digital sections 5, 6 of the circuit are better isolated than that taught in the prior art of that taught by Williams as well as an article of manufacture that is more easily produced.

Williams does not teach, disclose, or suggest the claimed invention. Williams teaches an article of manufacture that is much more costly to produce and that, as applicable to the article of manufacture claims, does not teach, disclose, or suggest the same structure.

Williams, as acknowledged in the Office Action includes a N+ buried layer. This buried layer requires that any substrate layer include a non-planar area for the buried layer and prevents the lower surface of an epitaxial layer and a top surface from being adjacent as now claimed.

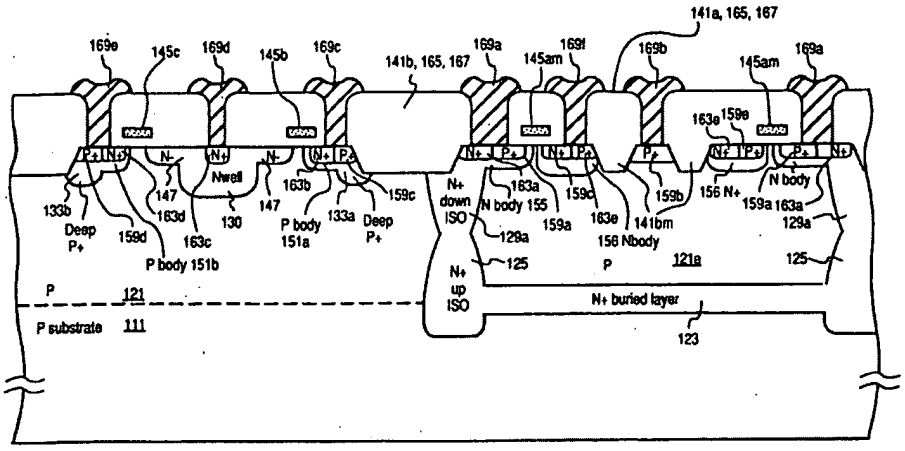


Fig. 25P

Williams includes the kinds of complexities that the prior art believed was necessary to achieve noise isolation. The Applicant's invention has greatly simplified the structure thereof and includes structure not found in Williams nor structure that is obvious given Williams.

Accordingly, the Examiner is respectfully requested to withdraw the rejection for this reason alone.

Moreover, the present invention provides an integrated circuit having a structure that includes a device isolation region that is not design to penetrate the epitaxial region. Thus, the presently claimed invention recites *"a device isolation region formed toward an inner part of the epitaxial layer from the top surface of the epitaxial layer between said first and second circuit sections."*

Williams teaches that the ISO 129a and 125 are N+ regions and that these are connected with source 169a of the LDMOS. See Fig. 25P. Therefore, the isolation between the P-type epitaxial layer 121 and the P-type epitaxial layer 121e is formed by a depletion layer due to a P-N junction. The depletion layer width, e.g., noise isolation effect, changes with changes in the voltage applied between the ISO 129a, 125 and the P-type epitaxial layer 121, 121e, e.g., bias condition. For example, when the voltage is small, the noise isolation effect is not sufficient.

In contrast in the presently claimed invention, the device isolation region comprises an insulating material which electrically separates between the digital section 5 and the analog section 6. Therefore, the noise isolation effect does not change with changes in the bias condition because of the absence of a depletion layer. Williams, alone or in combination with any other reference, fails to teach, disclose, or suggest this structure.

Accordingly, the Examiner is respectfully requested to withdraw the rejection for this reason alone.

Rejections in view of Crichi

Claims 1, 12, and 13 stand rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,559,349 to Crichi. Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Crichi.

The presently claimed invention includes the limitations:

> *"a silicon substrate having a substantially planar top substrate surface;*
> *a silicon epitaxial layer having a lower resistivity than the resistivity of said silicon substrate, the epitaxial layer having a substantially planar lower epitaxial surface, the epitaxial layer being formed upon the top substrate surface so that the lower epitaxial surface and the top substrate surface are adjacent;*
> *a first and a second circuit section formed in said silicon epitaxial layer, each circuit section spaced apart from the top substrate surface by a respective portion of the silicon epitaxial layer; and"*

As discussed above with respect to Williams, the presently claimed invention includes a specific structure wherein silicon substrate 2 includes a substantially planar top surface upon which an epitaxial layer is formed so that a substantially planar lower epitaxial surface and the top substrate surface are adjacent.

Crichi does not teach, disclose, or suggest the claimed invention. Crichi is alleged to teach a substrate 12, 14 and epitaxial layers 24, 32 as taught in Fig. 1 of the reference.

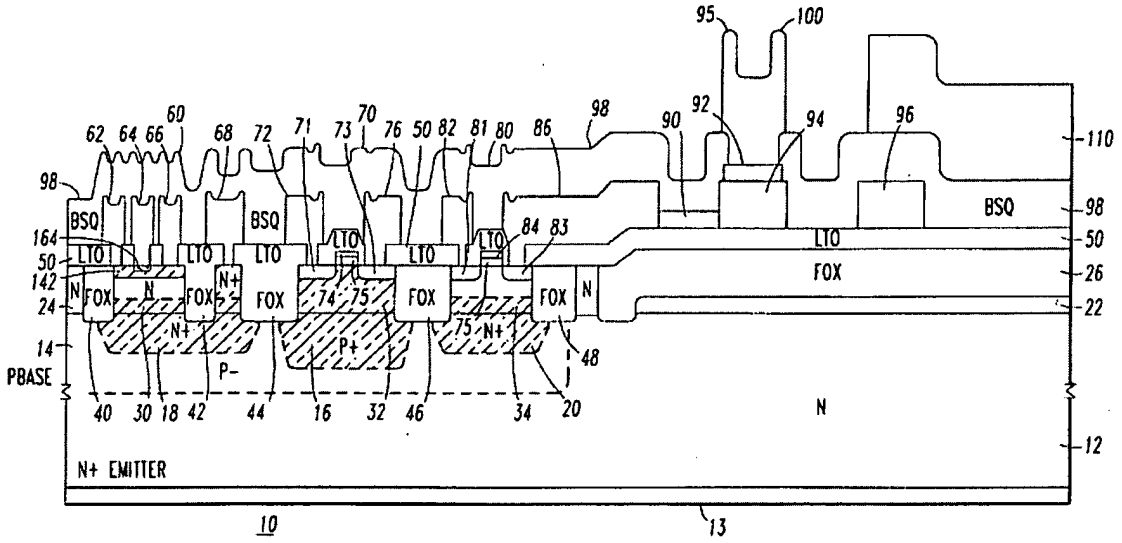


FIG. 1

However, as is apparent from Fig. 1, the alleged epitaxial layer and the alleged substrate layers are each interrupted by N+ and P+ wells 16, 18, 20. See 3: 1 et al. Thus, these layers do not teach, disclose, or suggest a substantially planar top substrate surface, a substantially planar lower epitaxial layer surface, and that these layers are adjacent while the circuits are spaced apart with respect to the substrate.

In fact, the use of wells as done by Crichi for noise isolation is extensively discussed by the Applicant in the application. For example, Figs. 2a and 2b illustrate the type of well structure advocated by Crichi. See 3:10-24 in the present application. However, using well structures are disadvantageous because of the costs involved and the complexity in making these. The present invention's simpler structure is far more cost effective than either the prior art illustrated in Figs. 2a and 2b or Crichi.

Accordingly, the Examiner is respectfully requested to withdraw the rejection for this reason alone.

Moreover, the present invention provides an integrated circuit having a structure that includes a device isolation region that is not design to penetrate the epitaxial region. Thus, the presently claimed invention recites *"a device isolation region formed toward an inner part of the epitaxial layer from the top surface of the epitaxial layer between said first and second circuit sections."*

Crichi teaches a P+ region in the epitaxial layer 32 extending to the P-type substrate 14. See Fig. 1. Similarly, an N+ region in epitaxial layer 34 extends to P-type substrate 14. These extended regions 16 and 20 are not separated by the isolation region of the FOX 46. This results in ineffective noise isolation.

In contrast, in the presently claimed invention, the device isolation region separates between the digital section 5 and the analog section 6. This results in effective noise isolation. Crichi, alone or in combination with any other reference, fails to teach, disclose, or suggest this structure.

Accordingly, the Examiner is respectfully requested to withdraw the rejection for this reason alone.

Rejections in view of Williams and Crichi

Claims 2, 3, and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Williams in view of Crichi.

As discussed above, Crichi and Williams both lack the essential teachings related to a substantially planar top substrate surface, a substantially planar lower epitaxial layer surface, and that these layers are adjacent while the circuits are spaced apart with respect to the substrate. Thus, one could not stand in for the gaps in the other and the combination of art.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this

application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Respectfully submitted,

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